REMARKS

Claim Rejection 35 U.S.C. § 112

The Examiner has rejected claims 10 and 14 under 35 U.S.C. 112, second paragraph as being indefinite for failing to particularly point out and distinctly claims the subject matter which Applicant regards as the invention. Applicant has amended claims 10 and 14 to more particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant, therefore, respectfully requests the removal of the 35 U.S.C. § 112 rejections of these claims.

Claim Rejections - 35 U.S.C. § 102/103

The Examiner has rejected claim 31 under 35 U.S.C. § 102(e) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Avanzino et al. (US Patent 6,140,239).

It is the Examiner's position that Avanzino teaches that a dielectric layer may be formed over a substrate and that the dielectric layer may have trenches therein. A barrier may be formed in the trenches and on a tope surface of the dielectric layer. Metal may be deposited over the barrier. The metal (such as copper) may be polished with a slurry. A slurry includes an abrasive. Dielectric layer may comprise an oxide of silicon. The barrier is electrically conductive, such as tantalum or tantalum nitride. It is the Examiner's position that Avanzino (Col. 4, lines 10-11) also teaches that the abrasive may comprise iron oxide.

It is the Examiner's position that the instantly claimed invention differs from Avanzino by specifying the slurry may includes an abrasive harder than the metal and less harder than the barrier. It is, however, the Examiner's position that because the same materials are used with the same process steps, it would inherently contain the same properties and functions as claimed, the abrasive harder than the metal (such as copper) and less harder than the barrier (such at tantalum or tantalum nitride).

After CMP of copper, it is the Examiner's position that Avanzino also teaches that subsequently, CMP is conducted to remove barrier layer from the upper surface of the dielectric layer leaving the planarized surface (Col. 5, lines 43-47). Avanzino also states that a slurry containing iron oxide enables effective planarization to achieve a smooth surface without abrasive. Therefore, slurrying containing iron oxide may be used to polish the barrier layer. Furthermore, it is the Examiner's position that during CMP of copper, because CMP (etch) process does not stop instantaneously, and the copper layer is harder than the barrier layer, therefore a portion of the soft barrier layer would have been inherently removed.

It is Applicant's understanding that the cited references fail to teach or render obvious Applicant's invention as claimed in claim 31. In claim 31, Applicant claims a method of forming an interconnect wherein a barrier layer is formed over and into trenches formed in a hard dielectric layer. A metal layer is then deposited over the barrier layer. The metal layer is then polished with a slurry that includes an abrasive which is harder than the metal and less hard than the barrier layer. After removing the metal layer by polishing and exposing the barrier layer on the top surface of the dielectric, the barrier layer on the top surface of the dielectric is polished utilizing the same slurry used to polish the metal layer. By utilizing a slurry having an abrasive that is harder than the metal layer but less hard than the barrier layer and wherein the dielectric layer is formed of a material having a hardness similar to the barrier layer, then the same slurry can be utilized to remove the barrier layer from the dielectric as is used to remove the metal layer from the barrier layer.

It is Applicant's understanding that Avanzino teaches to utilize two different CMP processes. The first CMP process is utilized to remove copper layer 20 from barrier layer 14 (Col. 5, lines 34-47). The first CMP process stops on barrier 14 as shown in Figure 3 (Col. 5, lines 44-45). After the first CMP process the substrate is cleaned of residual iron particles with a dilute organic acid (Col. 5, lines 39-43). After stopping on barrier layer 14 and cleaning the substrate of residual iron oxide, a second CMP process is used to remove barrier layer 14 from the upper surface of the interlayer dielectric layer 10 leaving a planarized surface as shown in Figure 4 (Col. 5, lines 44-47). As such, Avanzino clearly fails to teach removing the barrier layer 14 with the same slurry as utilized to remove copper layer 20.

Additionally, it is to be appreciated that one of ordinary skill in the art would not be motivate to utilize the slurry containing iron oxide used to polish copper layer 20 to polish

barrier layer 14 because Avanzino specifically teaches to clean the substrate to remove residual iron oxide (i.e., remove remaining portion of the first slurry) prior to polishing the barrier layer. If Avanzino envisioned or contemplated utilizing a slurry containing iron oxide to polish barrier layer 14, he certainly would not have suggested or taught to remove the residual iron oxide prior to polishing the barrier layer as he has done. Additionally, contrary to the Examiner's statement, in Applicant's claimed invention, the barrier layer is harder than the metal layer being polished. In Avanzino, slightly over polishing the soft copper layer 20 would not necessarily result in polishing of the harder barrier layer 14 let alone result in the complete removal of the barrier layer as claimed by Applicant. As such, for the above mentioned reasons, it is Applicant's understanding that Avanzino fails to teach or render obvious Applicant's invention as claimed in new claim 31.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

10. (Amended) The method of Claim [9] **1**, wherein the slurry has a pH in the range of 3.5 to 7.

14. (Amended) The method of Claim [13] **11**, wherein the abrasive comprises approximately 0.5 to 10 wt.% of the slurry.

31. (Amended) A method of forming an interconnect comprising:

forming a hard dieletric layer over a substrate, the dielectric having trenches therein;

forming a barrier in the trenches and on top of the surface of the hard dielectric layer;

depositing metal over the barrier;

polishing the metal with a slurry that includes an abrasive harder than the metal and less hard than the barrier; and

polishing said barrier from the top surface of said hard dielectric layer with said slurry **until said barrier is removed from the top surface of said hard dielectric layer**.